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(54) **Transconductor stage with controlled gain**

(57) A controlled gain transconductor (20) which comprises a transconductance stage (3) having at least two input terminals (I1, I2) and at least two output terminals (O1, O2), an active load (4) connected to the output terminals of the transconductance stage and a control circuit (5) for the active load (4) conneccted between said output terminals (O1, O2) and the active load (4).

Also provided is a circuit portion (10) being a replica of the transconductance stage (3), the active load (4) and the control circuit (5). This replicated portion (10) has an output connected to the control circuit (5) of the transconductor (20) to provide a predetermined voltage value (Vc) required for adjusting the DC gain of the device.

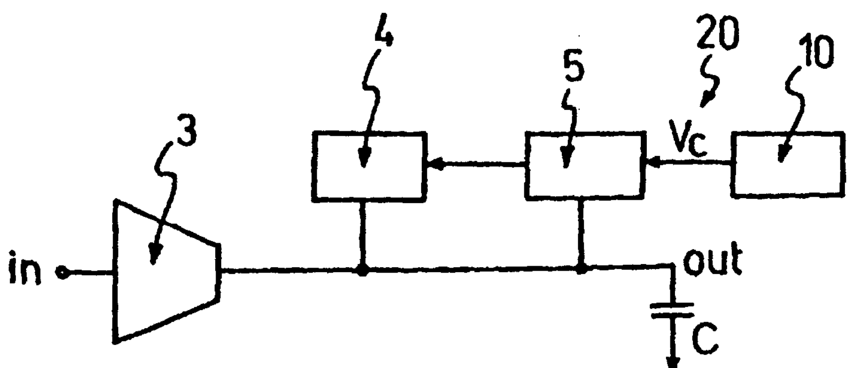

FIG.5

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Description

Fi ld of the Invention

This invention relates to a controlled gain transconductor comprising a transconductance stage connected between a first, supply voltage reference and a second voltage reference, with at least two input terminals and at least two output terminals.

The invention concerns in particular, but not exclusively, the implementation of filter integrators, and the description which follow will make reference to that application for convenience of illustration.

Background Art

A transconductor is basically a voltage-controlled, transconductance differential stage. It is used to implement integrators and active filter components, as well as oscillators and impedance transform circuits.

A practical integrator, as shown generally at 1 in Figure 1, for example, usually comprises a transconductor stage 2 having a finite output resistance R0 connected in parallel with a load capacitance C.

The transfer function FdT of the integrator 1, i.e. the ratio of the Fourier's transform of the output voltage signal Vo to the Fourier's transform of the input voltage signal Vi is given by the following expression:

$$FdT = Vo/Vi = gm^*R_0/(1 + j^*\omega^*R_0^*C) \qquad (1)$$

where gm is the transconductance of the transconductor 2.

The presence of even a low-value output resistance R0 makes the integrator 1 an approximate one by introducing a gain $A=gm^*R_0$.

Respectively denoted by the references A and B in Figure 2 are the frequency responses of an ideal integrator and of a real, i.e. approximate, integrator. It can be seen from the Figure that the frequency response from the real integrator shows damping at low values of the pulsation ω. The phase of the transfer function FdT of a real integrator 1 is:

$$\phi(\omega) = -\text{arctag } \omega^*R_0^*C = -\text{arctg } \omega/\omega_D \qquad (2)$$

where $\omega_D=1/(R_0^*C)$ is the pulsation corresponding to a gain $A=gm^*R_0$.

At the operating pulsation, as designated ω_o and equal to the gm/C ratio, the phase ϕ has the following value:

$$\phi(\omega_o) = -\text{arctg } \omega_o/\omega_D = -\text{arctg } A \qquad (3)$$

Taking into consideration the effect of a second equivalent pole as well, which is present at an equivalent pulsation of ωp and added to the pole of the ideal transconductor at the operating pulsation ω_o, the transfer function of the integrator 1 may be written as:

$$Fdt = Vo/Vi = A/((1 + j^*\omega/\omega_D) * (1 + j^*\omega/\omega_p)) \qquad (4)$$

where $A=gm^*R_0$ is the gain of transconductor 2 and $\omega_D=1/(R_0^*C)$ is the corresponding pulsation to that gain.

The phase overflow of the integrator 1 is defined, at the operating pulsation ω_o, by the difference:

$$\Delta\phi = \phi(\omega_o) - (-\pi/2) \qquad (5)$$

Simple mathematical calculations yield the relation:

$$\Delta\phi = \text{arctg } (\omega_D/\omega_o) - \text{arctg } (\omega_o/\omega_p)$$

$$= \text{arctg } [(1/A - \omega_o/\omega_p)/(1 + 1/A^*\omega_o/\omega_p)] \qquad (6)$$

For gains A much greater than 1 and second pole pulsations ω_p which are far apart from the operating pulsation ω_o, the relation (6) is brought to the following form:

$$\Delta\phi = \text{arctg } (1/A - \omega_o/\omega_p) \qquad (7)$$

This relation (7) shows that the phase overflow $\Delta\phi$ is affected by both the variation of gain A and the frequency position of the second equivalent pole, i.e. the pulsation ω_p.

Shown in Figure 3 is the frequency response (or Bode's Diagram) of a generic approximate integrator having a gain A and a second pole at pulsation ω_p (curve I).

Curve II in Figure 3 illustrates the frequency response from the same integrator when a phase overflow occurs due to a variation in gain (from A to A'), and curve III illustrates the frequency response from an integrator wherein the gain A and the second pole ω_p vary by the same amount in percent.

Curve III shows the same phase overflow $\Delta\phi$ as curve I at the operating pulsation ω_o.

Leaving out the contribution from the second pole at pulsation ω_p, the expression for the phase overflow $\Delta\phi$, at gains A well above unity, reduces to:

$$\Delta\phi = 1/A \qquad (8)$$

It can be appreciated from expression (8) that deviations of the gain A from a designed value result in variations of the phase overflow $\Delta\phi$ at the pulsation ω_o, with unity integrator gain.

Furthermore, where the integrator 1 is employed in the design of filters, the variations of the phase overflow may lower the accuracy of the so-called quality factor Q of a biquadratic cell -- an essential part to the implementation of filters, although not described herein because known per se.

Finally, the presence of a finite resistance R_0 brings about an attenuation in the input-output gain G of the above biquadratic cell.

Therefore, this gain error ΔG must be compensated for at the designing stage to provide the ideal gain sought.

In rder to restrain the phase overflows $\Delta\phi$ -- which, as previously mentioned, are inversely proportional to the gain A of the integrator 1 -- one could think of providing an integrator 1 having a particularly high gain A. In this way, variations in the gain A would induce phase overflows of negligible magnitude.

But his would actually imply a transconductor 2 design having high output resistances R_0, which is difficult to implement with certain high frequency technologies disallowing the use of transistors of the vertical pnp type.

The same problem is encountered when technologies for low supply voltages are employed, where PMOS transistors in a cascode configuration cannot be used for the active load.

A second design strategy currently employed provides for the designing of an integrator 1 with a low-value center or "nominal" gain, that is a controlled type of gain for deviations from its nominal value. In this way, those gain A variations on which the phase overflow $\Delta\phi$ is dependent can be cancelled as best as possible.

Moreover, with the gain limited to within two values, Amin and Amax, a biquadratic cell of a filter with the following "nominal" gain can be provided:

$$Anom = 2/(1/Amin + 1/Amax) \qquad (9)$$

thereby to achieve minimization of the gain error ΔG.

By employing low gain integrators and cells, simpler active loads and circuit topologies which operate on a low supply can be used.

To obtain a nearly constant gain A, the prior art has proposed that a load L be used which varies according to the variations in the transconductance gm of the transconductance stage 3.

This objective is attained by using a load L controlled by a voltage equal to A/gm, as explained by Baschirotto, Rezzi, Castello and Alini in "Design of High-frequency BiCMOS continuous-time filters with low-output impedance transconductor".

Since the transconductance of the stage 3 and the load L vary in the same direction, the gain A will not vary with such electrical parameters as the voltage and current levels.

A varying load L of transconductance g_L is provided by using CMOS complementary field-effect transistors. The transconductor 2 gain becomes:

$$A = gm/g_L = 2/\alpha \qquad (10)$$

where α is the fractional current flowing through the CMOS transistors that make up the load L.

As practiced, this solution fails to remove the gain variation with the process parameters that affect, in particular, the implementation of the complementary CMOS transistors. This solution also requires compensation circuitry, as described in European Patent Application No. 92830140.7 by the Applicant.

The technical problem which underlies this invention relates to the provisi n of a transconductor stage having such structural and functional features as to produce a controlled-gain integrator, regardless of operation or process conditions, thereby overcoming the above-mentioned limitations which beset the prior art.

Summary of the Invention

The solutive idea on which the invention stands is one of controlling the gain of the integrator, incorporating a transconductor, by varying the output resistance of the active load.

Based on this solutive idea, the technical problem is solved by a transconductor stage as indicated being characterized in that it comprises an active load controlled by a control circuit, said active load and said control circuit being connected to each other and to the outputs of the transconductance stage.

The features and advantages of a transconductance stage according to the invention will be apparent from the following detailed description of an embodiment thereof, to be taken by way of example only with reference to the accompanying drawings.

Brief Description of the Drawings

In the drawings:

Figure 1 shows an integrator with a transconductor incorporated thereto, according to the prior art;
Figure 2 shows respective ideal and real frequency responses from the integrator in Figure 1;
Figure 3 shows frequency responses from the integrator in Figure 1, when gain and pulsation variations of a second pole are encountered;
Figure 4 shows in greater detail a transconductor stage according to the prior art;
Figure 5 shows schematically a controlled gain transconductor embodying this invention;
Figure 6 shows in greater detail a portion of the transconductor in Figure 5;
Figure 7 shows an embodiment of the transconductor in Figure 5;
Figure 8 shows an embodiment of a replica circuit associated with the transconductor of Figure 5; and
Figure 9 shows schematically a portion of the replica circuit in Figure 8.

Detailed Description

With reference to the drawing figures, and to Figure 4 in particular, a conventional transconductor is shown generally and schematically at 2 which comprises a first or input circuit portion 20.

This input circuit portion 20 comprises a pair of n-channel MOS transistors M1 and M2 having their source

terminals S1 and S2 merged into a first common terminal X1.

The common terminal X1 is connected toward ground through a first gen rator A1 of a current Io.

The gate terminals G1 and G2 of the MOS transistors, respectively M1 and M2, form the input terminals I1 and I2 of the transconductor 2.

The first or input circuit portion 20 is connected to a second or output circuit portion 21 comprised of a pair of bipolar transistors T1 and T2.

Specifically, the drain terminals D1 and D2 of the MOS transistors M1 and M2 are connected to the emitter terminals E1 and E2 of the bipolar transistors T1 and T2.

The base terminals B1 and B2 of these bipolar transistors T1 and T2 are joined together into a second common terminal X2.

A diode D and a resistive bias element R, in series with each other, are connected between the second X2 and the first X1 terminals. To the second terminal X2, a second generator A2 of a current Id, referred to as the tuning current, is also connected.

The collector terminals C1 and C2 of the bipolar transistors T1 and T2 are the output terminals O1 and O2 of the transconductor 2 and connected to the drain terminals D3 and D4 of further MOS transistors M3 and M4, of the p-channel type, which are part of a third or bias circuit portion 22.

The transistors M3 and M4 are connected to each other into a current mirror configuration, with the terminals S3 and S4 connected to a supply voltage reference VD and the gate terminals G3 and G4 connected together into a third common terminal X3 which is applied a control voltage Vc.

As a first approximation, the expression for the gain A of the transconductor 2 in Figure 4 is as follows:

$$A = gm_{NMOS}/gds_{PMOS} \qquad (11)$$

where:

- gm_{NMOS} is the transconductance of the n-channel MOS transistors M1 and M2, as given by,

  $$gm_{NMOS} = I_M/[(Vgs - Vth) - Vds_{NMOS}/2)] \qquad (12)$$

  in which Vgs is the gate-source voltage, Vth is the threshold voltage, Vds_{NMOS} is the drain-source voltage of the transistors M1 and M2 themselves, and I_M is the current flowing therethrough;
- gds_{PMOS} is the drain-source conductance of the p-channel MOS transistors M3 and M4, as given by,

  $$gds_{PMOS} = \lambda * I_M/(1 + \lambda * Vds_{PMOS}) \qquad (13)$$

  in which λ is the channel modulation coefficient, Vds_{PMOS} is the drain-source voltag of the MOS transistors M3 and M4 themselves, and I_M is the current flowing through th transistors M1 and M2.

Since the voltage Vfs_{NMOS} of the transistors M1 and M2 is tied to the tuning current Id, the gain A is also bound to depend on this current.

On the other hand, Vds_{PMOS} is held constant by the circuit that sets the common mode output voltage.

Shown more schematically at 20 in Figure 5 is the controlled-gain transconductor of this invention.

The transconductor 2 comprises a transconductance stage 3, an active load 4, and a control circuit 5, as well as a capacitor C connected between the output of the transconductance stage 3 and a voltage reference, such as a signal ground (GND).

The active load 4 and control circuit 5 are connected in parallel between the output of the transconductance stage 3 and the capacitor C.

The active load 4 is implemented by a double load circuit 8, 9, specifically by a double pair of MOS transistors M13, M14 and M15, M16, all of the p-channel type.

Only one of the two transistor pairs is shown in Figure 6, namely pair 8 comprised of the transistors M13 and M14. The source terminals S13 and S14 are connected to the supply voltage reference V_D. The drain terminals D13 and D14 are connected to each other.

These MOS transistors, M13 and M14, have currents I_1 and I_2, respectively, flowed therethrough, and are characterized by different channel lengths L_1 and L_2.

The configuration in Figure 6 has a drain-source conductance gds given by:

$$gds = \lambda(L_1) * I_{M1}/(1 + \lambda(L_1) * Vds_{PMOS}) + \\ + \lambda(L_2) * I_{M2}/(1 + \lambda(L_2) * Vds_{PMOS}) \qquad (14)$$

A preferred embodiment of the circuit of transconductor 2 is shown in Figure 7, and comprises a transconductance stage 3 similar to the conventional one, with a feedback circuit 6 for the transconductor common mode signals connected to its output terminals O1 and O2.

The common mode feedback circuit 6 comprises a double differential cell, wherein a first cell comprises a first pair of MOS transistors M5 and M6 of the n-channel type which have their source terminals S5 and S6 in common and connected to a first current generator A3 supplying a current I_M.

The first MOS transistor M5 has its gate terminal G5 connected to the output O2 of the transconductance stage 3, whilst its drain terminal D5 is connected to the supply voltage reference V_D.

The second MOS transistor M6 has its gate terminal G6 connected to the gate terminal G7 of a first transistor M7 in a second MOS transistor pair M7 and M8, also of the n-channel type and included to the second cell.

The MOS transistors M7 and M8 have their source terminals S7 and S8, respectively, connected together and to a further current generator A4 which supplies the current I_M.

The gate terminal G8 of the second MOS transistor M8 in the second pair is connected to the first output terminal O1 of the transconductance stage 3, the drain ter-

minal D8 being connected to the supply voltage reference V_D.

The drain terminals D6 and D7 of th MOS transistors M6 and M7, respectively, are connected to a circuit 7 referred to hereinafter as the DC gain adjustment circuit. The common mode feedback circuit 6 and the adjustment circuit 7 are parts of the control circuit shown at 5 in Figure 5.

The adjustment circuit 7 comprises a first pair of MOS transistors M9 and M10, and a second pair of MOS transistors M11 and M12, all of the n-channel type.

The transistors M9 and M10 have their source terminals S9 and S10 connected together and to the drain terminal D6 of the MOS transistor M6 included to the common mode feedback circuit 6.

Likewise, the MOS transistors M11 and M12 have their source terminals S11 and S12 connected together and to the drain terminal D7 of the MOS transistor M7 included to the common mode feedback circuit 6.

The MOS transistors M9 and M12 have their gate terminals G9 and G12 connected together to provide a common terminal Y1, and their drain terminals D9 and D12 also connected together to provide a second common terminal Y2.

The MOS transistors M10 and M11 have their drain terminals D10 and D11 connected together to form a third common terminal Y3 and their gate terminals G10 and G11 connected together into a fourth common terminal Y4.

A control voltage Vc is applied between the terminals Y4 and Y1 of the adjustment circuit whose greater potential goes to the terminal Y4.

The terminals Y2 and Y3 are connected to a pair A of MOS transistors M_{1A} and M_{2A} of the p-channel type incorporated to a current mirror portion 5a, in turn included to the control circuit 5.

The gate terminal G_{1A} of the MOS transistor M_{1A} is connected to both of the transistor pairs, 8 and 9, incorporated to the active load 4 of the transconductor. More particularly, the terminal G_{1A} is connected to the gate terminals G14 and G15.

The gate terminal G_{2A} of the MOS transistor M_{2A} is also connected to both of the transistor pairs 8 and 9 incorporated to the active load 4 of the transconductor. In particular, this terminal G_{2A} is connected to the gate terminals G13 and G16.

The pair of p-channel MOS transistors M13 and M14 which form the first load circuit 8 of the active load 4 have their drain terminals D13 and D14 connected to the output terminal O1 of the transconductance stage 3.

The second pair of transistors M15, M16 forming the second load circuit 9 of the active load 4 have their drain terminals D15 and D16 connected to the second output terminal O2 of the transconductance stage 3.

The common mode feedback circuit 6 is selected to have at least the same linearity range for differential signals as the transconductance stag 3.

The operation of the transconductor 2 according to the invention will now be reviewed.

The common mode feedback circuit 6, as shown in Figure 7, sets the voltages at the output terminals O1 and O2 to a predetermined value Vcm.

Under this condition, the incoming currents I_1 and I_2 to the MOS transistors M6 and M7 will be:

$$I_1 = I_2 = I_M/2 \qquad (15)$$

The sum of the currents which are flowing through the transistors M_{1A} and M_{2A} will therefore be $I_1+I_2=I_M$.

By acting on the control voltage Vc, an equivalent drain-source conductance gds can be obtained as given by relation (14) above.

By virtue of the respective current mirror connections of the transistors M13; M16 and M15; M16 in the load circuits 8 and 9 to the MOS transistors M_{2A} and M_{1A} in the portion 5a, the overall active load of the transconductor 2 replicates the equivalent drain-source conductance gds of the transistor pair M_{1A} and M_{2A}.

The voltage Vc is generated by an appropriate replica circuit 10, shown in Figure 8.

The bias replica circuit 10 comprises a second transconductance stage 11, being actually a replica of the transconductance stage 3. It matters to observe, however, that this stage 11 is input a constant voltage value ΔV, not a signal voltage.

Load circuits 18 and 19, being replicas of the circuits 8 and 9, form an active load 14, and are respectively connected to outputs 13 and 14 of the transconductance stage 11.

The MOS transistors contained in the replica circuit 10 have been denoted by the same references as the corresponding MOS transistors in the circuit architecture of Figure 7, with an "R" suffix to indicate their replicated functions. Accordingly, circuit portions 15, 16, 17 are illustrated which fully correspond to the portions 5a, 6, 7.

The circuit 16 can be viewed, similar to circuit 6, as a common mode feedback circuit, and controls the common mode voltage Vcn of the transconductance stage 11.

A potential difference Vout exists between the outputs 13 and 14 of the transconductance stage 11 which will be referred to as the output voltage from the stage.

The replica circuit 10 further comprises a differential amplifier 12 having four inputs I3, I4, I5, I6 and two outputs 25, 26.

Shown in Figure 9 is a circuit embodying said differential amplifier 12 with four inputs.

The inputs I3 and I4 are respectively connected to the outputs 13 and 14 of the transconductance stage 11, whilst the inputs I5 and I6 receive a constant voltage value equal to ΔV*A, where A is the gain sought.

The output 25 of the differential amplifier 12 is connected to the gate terminals G15R and G16R of MOS transistors M12R and M9R, and the output 26 is connected to the gate terminals G10R and G11R of MOS transistors M10R and M11R.

The difference of the voltage at the output terminal 26 with respect to that at the output terminal 25 gener-

ates the control voltage Vc which is then applied across the terminals Y4 and Y1 of the adjustment circuit 7 in Figure 7.

The DC gain is s t by the feedback operational amplifier 12. The loop will be stable when the output voltage Vout from the second transconductance stage 11 equals the value ΔV*A. Thus, the target gain A can be provided.

Claims

1. A controlled gain transconductor which comprises a transconductance stage (3) having at least two input terminals (I1, I2) and at least two output terminals (O1, O2), characterized in that it comprises an active load (4) connected to the output terminals of said stage and a control circuit (5) for the active load (4) connected between said output terminals (O1, O2) and the active load (4).

2. A transconductor according to Claim 1, characterized in that said active load (4) comprises at least one a pair of transistors (M13, M14), each having first and second terminals (S13, S14, D13, D14) and a control terminal (G13, G14), the first (S13, S14) and second (D13, D14) terminals of said transistor pair being connected together, and the control terminals (G13, G14) being connected to the control circuit (5).

3. A transconductor according to Claim 1, characterized in that said active load (4) comprises first (8) and second (9) load circuits respectively connected between a supply voltage reference (VD) and a corresponding one of the output terminals (O1, O2) of the transconductance stage (3).

4. A transconductor acccording to Claim 3, characterized in that each load circuit (8, 9) comprises at least one pair of parallel-connected transistors (M13, M14; M15, M16) having respective control terminals (G13, G14; G15, G16) connected to respective outputs of the control circuit (5).

5. A transconductor according to Claim 2, characterized in that the transistors (M13, M14) in said at least one pair are of the p-channel MOS type.

6. A transconductor according to Claim 5, characterized in that the drain terminals (D13, D14) of said MOS transistors (M13, M14) are connected to a corresponding output terminal (O1) of the transconductance stage (3).

7. A transconductor according to Claim 1, characterized in that the control circuit (5) comprises: a first, common-mode signal feedback circuit (6) connected to the output terminals (O1, O2) of the transconductance stage (3); a second, DC-gain adjustment circuit (7) output connected to the feedback circuit (6); and a current-mirror circuit portion (5a) connected b tween the adjustment circuit (7) and the active load (4).

8. A transconductor according to Claim 7, characterized in that said first common-mode feedback circuit (6) comprises at least one pair of differential cells, each comprised of a pair of transistors (M5, M6; M7, M8) with at least one terminal (S5, S6; S7, S8) in common and connected to a current generator (A3, A4), the control terminal (G5, G8) of a transistor in each pair (M5, M8) being connected to a corresponding one of the output terminals (O1, O2) of the transconductance stage (3).

9. A transconductor according to Claim 7, characterized in that said second, adjustment circuit (7) comprises at least one transistor pair (M9, M10) having at least one terminal (S9, S10) in common and connected to the common-mode feedback circuit (6).

10. A transconductor according to Claim 1, characterized in that it comprises a circuit portion (10) being a replica of said transconductance stage (3), said active load (4) and said control circuit (5), which circuit portion has an output connected to the control circuit (5) of the transconductor.

11. A transconductor according to Claim 10, characterized in that said replicated circuit portion (10) comprises a second transconductance stage (11) being a replica of said stage (3) and having a constant voltage applied to its inputs.

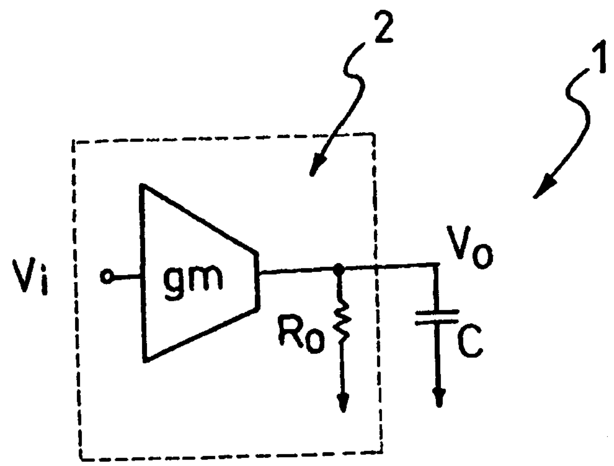
12. A transconductor according to Claim 10, characterized in that said replicated circuit portion (10) further comprises a differential amplifier (12) with four inputs (I3, I4, I5, I6) and two outputs (25, 26), the first two inputs (I3, I4) of said amplifier (12) being connected to the outputs (13, 14) of the second transconductance stage (11) and the second inputs (I5, I6) of the amplifier (12) being applied a constant voltage.

13. A transconductor according to Claim 10, characterized in that, within said replicated circuit portion (10), the control circuit comprises: a first, common-mode signal feedback circuit (16) connected to the output terminals (13,14) of the second transconductance stage (11); a second, DC-gain adjustment circuit (17) output connected to the feedback circuit (16); and a current-mirror circuit portion (15) connected between the adjustment circuit (17) and the replicated active load (14).

14. A transconductor according to Claim 12, characterized in that the outputs (25, 26) of said amplifier (12) are connected to said second adjustment circuit (17)

and the control circuit (5) to provide a predetermined voltage valu (Vc).

15. A transconductor according to Claim 10, characterized in that said second transconductance stag (11) has a transconductance (Gm) whch is regulated by a bias current equal to that supplied to said first transconductance stage (3).



PRIOR ART

FIG.1

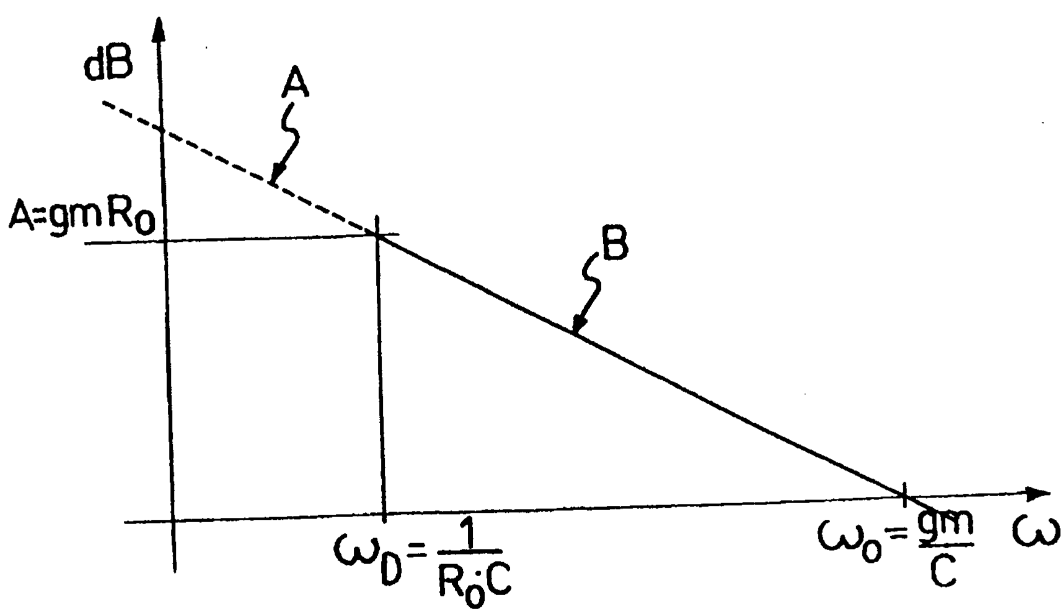
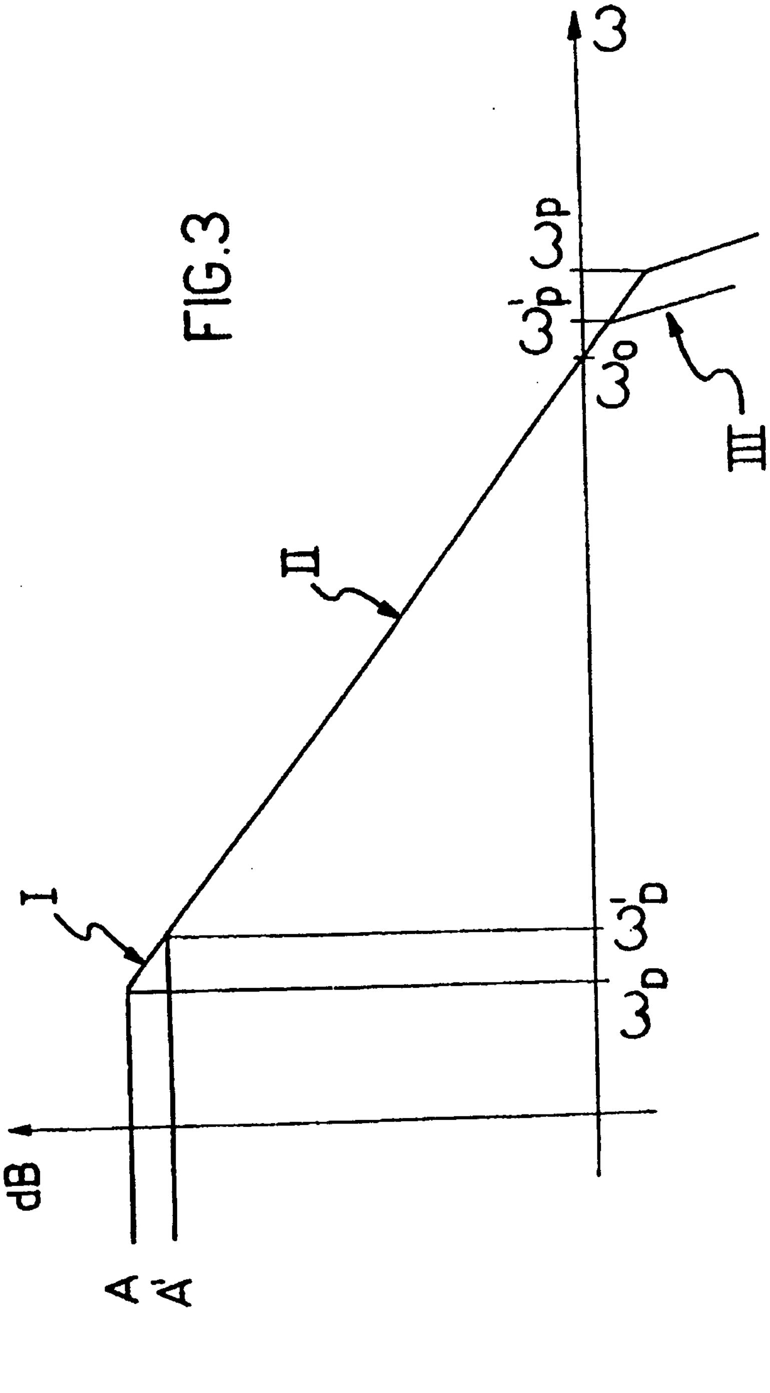
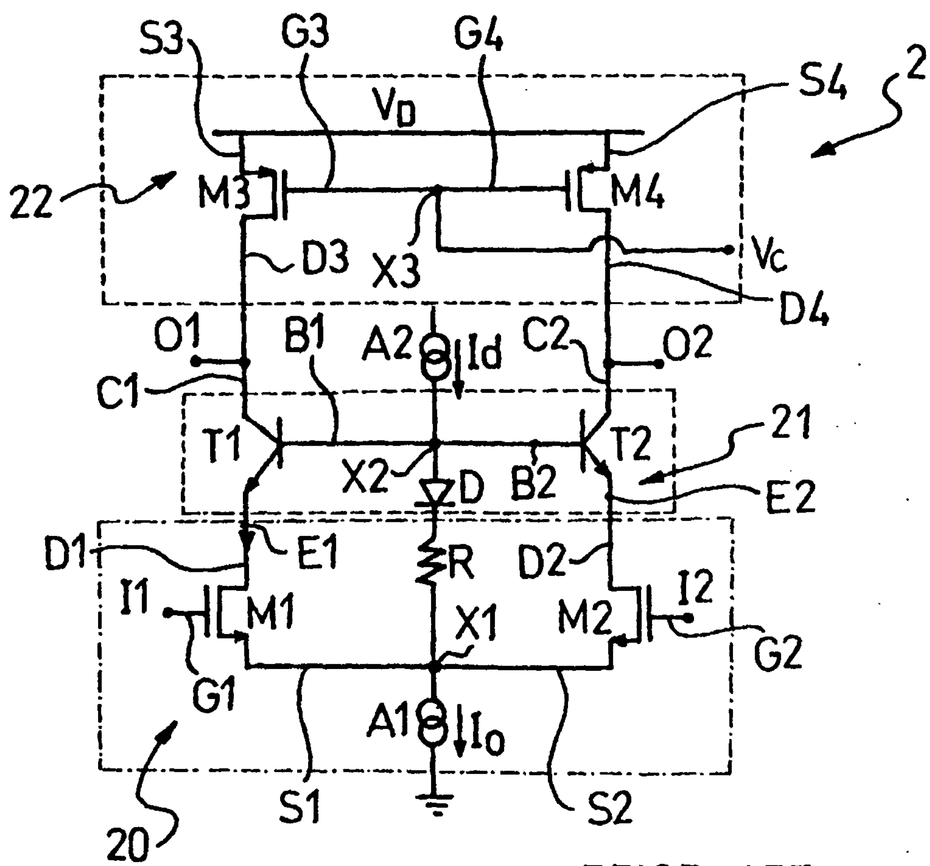


FIG.2

FIG.3





PRIOR ART

FIG.4

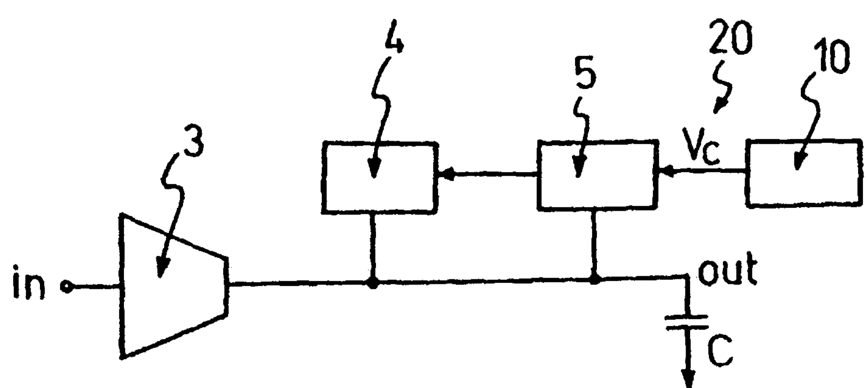


FIG.5

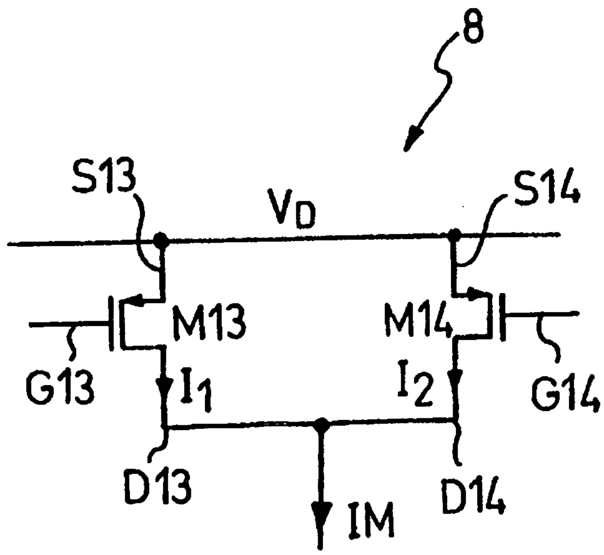
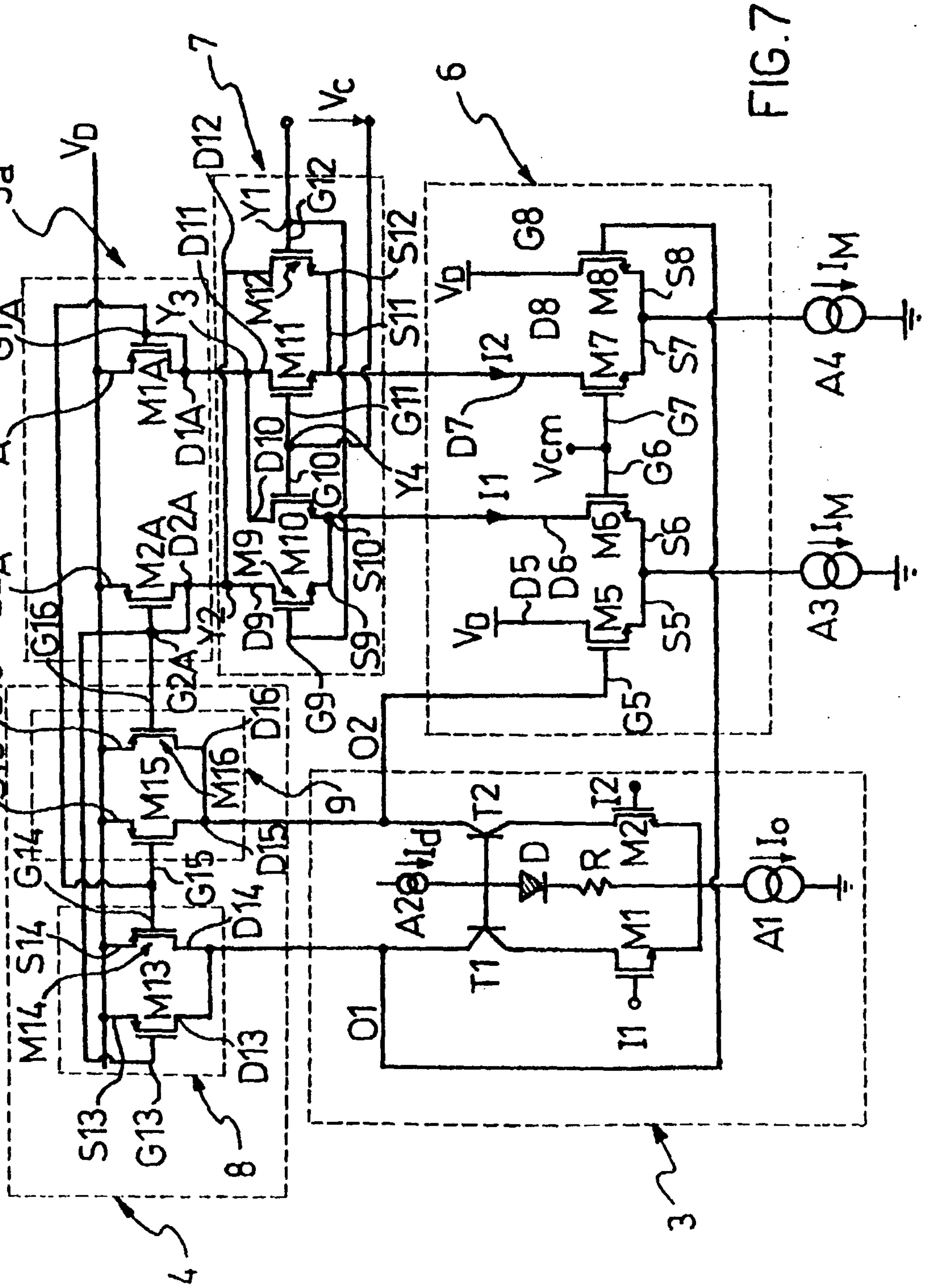


FIG.6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VD
7
Vc
6
4
3
8
9
M1A
M2A
M9
M10
M11
M12
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M14
M15
M16
M5
M6
M7
M8
M1
M2
T1
T2
D
R
A1
A2
A3
A4
Io
Id
IM
I1
I2
Vcm
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Y1
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G13
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D14
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D16

FIG.7

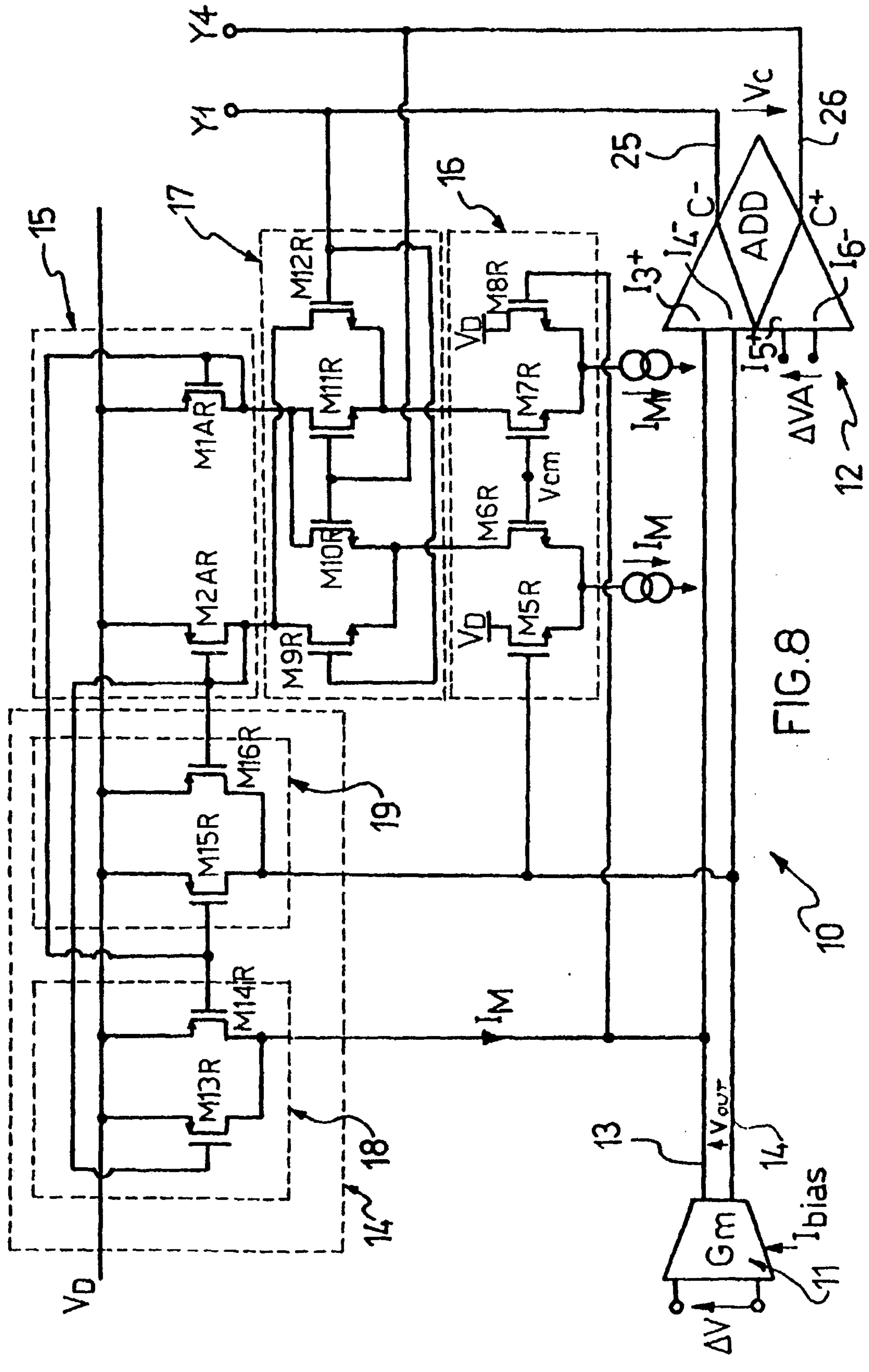
Y4
Y1
Vc
26
25
C-
ADD
C+
I4-
I3+
I5+
I6-
ΔVA
12
16
17
15
M12R
M11R
M8R
VD
M7R
IM
Vcm
M6R
M5R
M10R
M9R
M1AR
M2AR
M16R
M15R
19
M14R
M13R
18
14
13
Vout
Gm
Ibias
11
ΔV
10

FIG.8

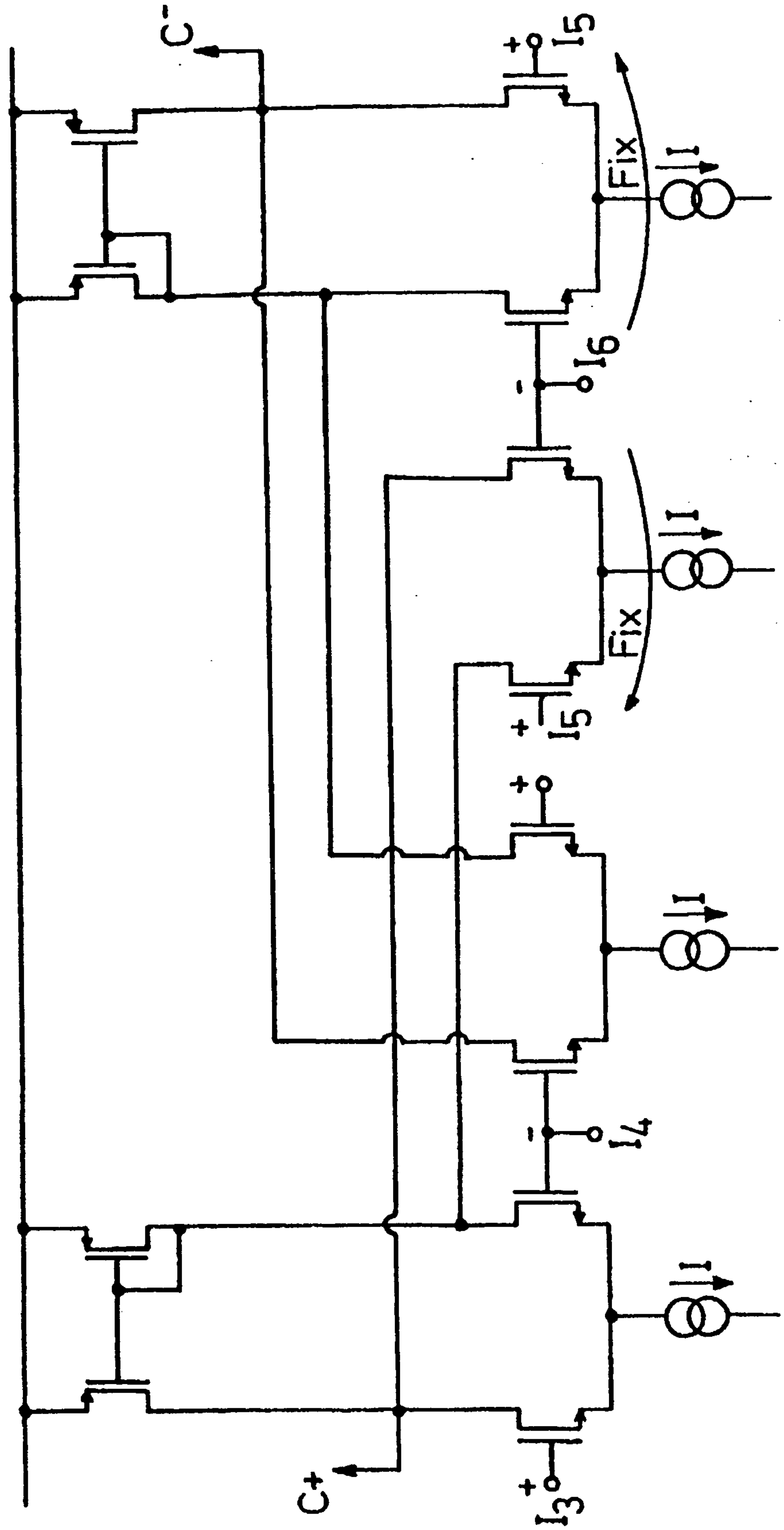

FIG.9

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0390

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 390 (E-813) 29 August 1989 & JP-A-01 137 810 (TOKO INC) * abstract *	1	H03G1/00 H03F1/08 H03H11/04
D,A	EP-A-0 561 099 (SGS - THOMSON) * abstract *	1	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.SC-20, no.6, December 1985, NEW YORK US pages 1144 - 1150 J. H. HUIJSING ET AL. 'Low - Voltage Operational Amplifier with Rail - to - Rail Input and Output Ranges'		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03F H03H H03G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 December 1994	Blaas, D-L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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